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☐ 1. Document ID: US 6373848 B1

L2: Entry 1 of 1 File: USPT Apr 16, 2002

DOCUMENT-IDENTIFIER: US 6373848 B1
TITLE: Architecture for a multi-port adapter with a single media access control (MAC)

US Patent No. (1):
6373848

Brief Summary Text (6):
What is needed is a multi-port adapter fabricated as a chip having a reduced number of gates. Lowering the gate count reduces the cost of the chip both when it is a stand alone chip and when it is a macro integrated into a larger chip.

Brief Summary Text (17):
Another object is a multi-port adapter chip and method of operation having a reduced MAC circuit count.

Detailed Description Text (13):
When the complete preamble has been transmitted to the PHY layer, (byte count=7) the state machine will transmit the SFD (Start Frame Delimiter) and move to the "DATA" state. If a media Collision occurs while the state machine is in the "Preamble" state and the PHY is able to accept a frame byte, the state machine will transfer to the "JAM" state. If the PHY cannot accept a frame byte, the state machine will go to the "JAM Wait" state and wait until the PHY is ready to accept more data. If a collision was not detected and the PHY is not ready to accept more data, the state machine will send the SFD and go to the "WAIT" state where it will remain until the PHY can accept more data.

Detailed Description Text (39):
Col 7 l 50 The "GAP" state is used to place the MAC logic in a state where it will not attempt to receive another frame for at least four clock cycles after the previous frame is received. The signal "Filter_Period" is generated by a counter and counts from zero to three. After the four cycles have elapsed, the state machine returns to the "IDLE" state where it is ready to receive the next frame.

Detailed Description Text (48):
Col 8 l 35 The "DATA" state is the state where data is taken from the TxFIFO and sent to the media. When the Control Logic 34 starts a transmit operation, it provides the TxMAC with the frame byte count. This byte count is used to determine when the complete frame has been transmitted. If the byte count is not equal to zero and the transmit is "active", the data byte that has been removed from the TxFIFO is presented to the TxMII for transmission. The TxFIFO data address is incremented, and the byte count is decremented. Both are placed back into the Transmit state register 26 until this

port is serviced again.

Detailed Description Text (49):
When the byte count is equal to zero, a Reset to the TxMII is asserted. This will notify the TxMII that the complete frame has been sent and the CRC should be appended to the frame. The state machine will go to the "CRC" state to transfer the CRC to the TxMII logic.

Detailed Description Text (50):
If a Collision is detected on the media, the byte count is checked to determine if the collision is an Early collision. If the byte count is 64 or less, the collision is early and transmission of the frame is stopped with a JAM sequence. The TxFIFO address is returned to the beginning of the frame and the state machine goes to state "IFG" to produce the Interframe Gap. The indication that a frame is in the TxFIFO remains set and the frame will be retransmitted when the IFG expires. If the byte count is greater than 64 when the collision occurs, the TxMII logic is instructed to send the JAM sequence and stop the frame transmission. The Control Logic 34 is instructed that the frame has been transmitted. The frame is not retransmitted.

Detailed Description Text (52):
This state is entered after all of the frame data has been transmitted, indicated by a byte count of zero. The CRC is four bytes in length and the state machine will remain in the "CRC" state until all four bytes of the CRC have been sent to the TxMII logic. When all four bytes of the CRC have been sent, the state machine will go to the IFG state.

Detailed Description Text (65):
The port selector 46 is coupled to the multiplexer 18 and the state registers 26 and 30. The port selector is a free-running counter whose output selects the current port to logically attach to the MAC. The port selector counts ports minus 1 from 0 to N and wraps back to 0. N is the number of ports minus 1 in the implemented design. For a 10 port design, the port selector would count from 0 to 9 returning to 0 and repeating the sequence. The output of the port selector is used to control the multiplexer 18 and is also used to select one of the transmit state registers 26 and 30. The process of selection of the state registers and selecting the port is synchronous and is controlled by the port selector.

Detailed Description Text (68):
Data is passed from the interfaces 20 and 22 to the MAC logic 24 and 28, respectively, via an 8-bit bus. Therefore, for 100 mbps operation, an 8-bit word of data is available every 80 nanoseconds. If the desired number of ports is 10, the internal clock of the chip can be run with 8 nanosecond cycles. The port selector implemented as a cyclic counter ranges from 0 to 9 or can be implemented to select ports based on a priority or service needed algorithm. In each cycle, a different port is selected. The registers containing state information and frame processing status are replicated for each port. The port selector 46 is used to swap in the state information for the appropriate port to allow cycle processing of that port. At the end of the cycle, the registers are set and stay set until selected again. This process repeats for each port. Once data is accumulated in the receive FIFO or space is available on the transmit FIFO, control information is presented to control logic 34 serving both ports. The control logic will then read or write data from the appropriate FIFO partition to or from the host or network, as the case may be.

Detailed Description Text (77):
Summarizing, the present invention describes a multi-port adapter having a single MAC to transfer data in both directions between a host system and a communication network operating on a TDM basis. The MAC has a receive path and a transmit path for processing TDM frames after preliminary processing by a transmit and receive interface, respectively. A port selector selects a register of a state machine for determining the state of the MAC to process data from a selected port. The state machine also identifies a section of a transmit and receive FIFO for storing data in or moving data to the network. The MAC units write the specific address of the data in the FIFO's. Control information is provided by the FIFO's to control logic to transfer data from the receive FIFO to the host system once data is accumulated and

transfer data from the transmit FIFO to the network once space is available in the FIFO. The single MAC reduces the circuit count for the adapter as compared to prior art devices using multiple MACs for transferring data.

Full | Title CLS.1 REF.1 SEQ.1 ATT.1

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Term	Documents
COUNT$	0
COUNT.USPT.	167063
COUNTA.USPT.	22
COUNTABILITY.USPT.	9
COUNTABLE.USPT.	744
COUNTABLE-PULSE.USPT.	2
COUNTABLE/UNCOUNTABLE.USPT.	1
COUNTABLY.USPT.	24
COUNTABLY-CODED.USPT.	1
COUNTABLY-SEQUENCED.USPT.	1
COUNTACCESSOR.USPT.	3
(L1 AND (COUNT$)).USPT.	1

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☐ 1. Document ID: US 6373848 B1

L2: Entry 1 of 1 File: USPT Apr 16, 2002

DOCUMENT-IDENTIFIER: US 6373848 B1
TITLE: Architecture for a multi-port adapter with a single media access control (MAC)

Abstract Text (1):
A multi-port adapter having a single MAC chip has reduced logic circuits for transferring data between a host system and a TDM communication system. The MAC chip includes a transmit MAC and a receive MAC, each coupled at one end to a port multiplexer through an interface and at the other end to respective storage registers. The port multiplexer is coupled to the Physical Layer of each port. Transmit and receive state registers track the state of each port in the transfer of data in the transmit and receive directions. The storage registers are coupled through a host bus interface to a host bus and to the host system. Control logic is coupled to the storage register to control the transfer of data between the system and the storage registers. A port selector coupled between the multiplexer and the transmit and receive state registers selects ports for transfer of data in succession. On each chip clock cycle, the port selector selects a state machine register to determine the state of the MACs for processing the data and a section of the FIFO's to write or read data for the selected port. At the end of the cycle, the state registers are set and stay set until selected again. The process repeats for each port in a cyclic manner. Once data is accumulated in the receive storage register, control logic reads the data of the host bus. Once space is available in the transmit storage register, the control logic writes data from the host system to the transmit storage register.

Brief Summary Text (8):
U.S. Pat. No. 5,568,476 issued Oct. 22, 1996, discloses a single MAC serving multiple ports using a transmit MAC, a transmit buffer, a receive MAC, a receive buffer, a control logic for reserving storage in the buffer for transmitted and received data.

Brief Summary Text (13):
U.S. Pat. No. 5,355,375 issued Oct. 11, 1994, discloses a hub controller for providing deterministic access to Carrier-Sense-Multiple-Access (CSMA) Local Area Network. The hub controller includes media control logic that can selectively raise a pseudo-carrier control signal to each port thereby inhibiting any CSMA/collision detection protocol LAN transmissions by that port. In this way, the media control logic allows the hub controller to control which of the multiple ports will be allowed to contend for access to a common internal bus within the hub controller and for how long.

Brief Summary Text (21):

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These and other objects, features and advantages are achieved in a multi-port adapter chip having a single MAC coupled between a host system and a multi-channel network. The single MAC includes a transmit MAC and a receive MAC path. Each path is coupled at one end through a Media Independent Interface (MII) to a multiplexer and at the other end to separate transmit and receive storage (FIFO) devices. A transmit state machine is coupled to the transmit MAC and transmit FIFO. A receive state machine is coupled to the receive MAC and receive FIFO. The multiplexer is coupled to each port serving a channel through a register and a Physical Layer. Each FIFO is coupled to a host interface and provides instructions to control logic for transmitting and receiving data between the host system and the network. A port selector is coupled to the multiplexer and to the transmit and receive state machines for selecting each port on a cycle basis to transmit and receive data. Each state machine contains a state table having a one word entry for each port in tracking the status of the port. As the ports are selected by the port selector, the associated word for a port is read from the table and used to control the state machine in servicing the port. The port selector also assigns a section in the FIFO's for storing data processed or to be processed by the MACs. The transmit and receive state machines operate concurrently and determine the MAC state for servicing the port, after which the MAC state is updated and stored back into the state table. In the receive direction, the ports are serviced in a round robin fashion. In the transmit direction, data is written into the transmit FIFO as space becomes available. Control Logic means controls the transfer of data between the host system and the network and vice-a-versa when instructed by the FIFOs. The chip architecture is extendable from 10 mbps to 100 mbps and reduces the chip logic by approximately 75% compared to prior art devices.

Detailed Description Text (4):
The transmit interface 20 (TxMII) is coupled to a transmit MAC 24 (TxMAC) in the transmit path 19. The transmit MAC is coupled to a storage device 40, typically a FIFO (TxFIFO) through control 42 and data 44 lines. The device 40 stores data received from the host interface 16 under control of control logic 34. A transmit state register and multiplexer 26 exchanges data with interface 20, the MAC 24 and the storage device 40 under the control of a port selector 30, as will be described hereinafter.

Detailed Description Text (5):
Similarly, the receive interface (RxMII) 22 is coupled to a receive MAC (RxMAC) 28 in the receive path 21 which in turn is coupled to a receive storage device 43, typically a FIFO (RxFIFO) through control 36 and data lines 38. The device 43 stores data received from the host interface 16 under control of the control logic 34. A receive state register and multiplexer 23 exchanges data with the interface 22, the MAC 28 and the storage device 42 under the control of the port selector 30, as will be described hereinafter.

Detailed Description Text (7):
Returning to FIG. 1, the transmit interface 20 transmits the Preamble and Start Frame Delimiter; calculates the frame Cyclic Redundancy Check (CRC) and signals errors to the Physical Layer. The transmit interface 20 interfaces to the multiplexer 18 in such a way that the logic of the interface 18 behaves just as though it were connected directly to the Physical Layer of a channel. In this way the transmit interface 20 is identical to a single port MAC design. In FIG. 3, a state diagram describes the operations of the transmit interface in transmitting the preamble; Start Frame Delimiter; Calculating the Frame CRC; and identifying signalling errors to the physical layer. The multiplexer 18 provides the following signals to the TxMII state machine; COL (collision) which indicates a collision was detected on the media, and Tx_BC is a signal that indicates that the associated PHY layer can accept a byte of data in the TDM time slot. The signal "Active" is a signal from the control logic 34 that indicates that a frame is ready to be transmitted.

Detailed Description Text (11):
Frame transmission states when the state machine is in the "IDLE" state and the control logic 34 asserts the active signal. The state machine will remain in the "IDLE" state until it receives a signal from the PHY indicating the PHY can accept a byte of information. This ability to accept information is conveyed via the TX_BC signal. If the PHY is able to accept a byte, the state machine advances to state "PREAMBLE". If the PHY is unable to accept a byte, the state machine remains in the "IDLE" state.

Detailed Description Text (27):
The RxMII state machine flow controls the logic used to accept frames received from the media and transferred from the PHY layer to the MAC logic. The state machine is used to strip the Preamble, search for the SFD to establish byte sync and then strip the SFD, and accept the frame payload.

Detailed Description Text (46):
FIG. 5 is a state diagram of a typical TxMAC. The state machine is placed into the "IDLE" state when it receives a Power-on_Reset (POR). When the Control Logic 34 detects that a frame or partial frame is in the Tx FIFO, it will notify the TxMAC to start the transmission of this frame by asserting the "Active" signal. Until the "Active" signal is received, the TxMAC state machine remains in the "IDLE" state. When the "Active" signal is received, the state machine goes to the "DATA" state.

Detailed Description Text (48):
The "DATA" state is the state where data is taken from the TxFIFO and sent to the media. When the Control Logic 34 starts a transmit operation, it provides the TxMAC with the frame byte count. This byte count is used to determine when the complete frame has been transmitted. If the byte count is not equal to zero and the transmit is "active", the data byte that has been removed from the TxFIFO is presented to the TxMII for transmission. The TxFIFO data address is incremented, and the byte count is decremented. Both are placed back into the Transmit state register 26 until this port is serviced again.

Detailed Description Text (50):
If a Collision is detected on the media, the byte count is checked to determine if the collision is an Early collision. If the byte count is 64 or less, the collision is early and transmission of the frame is stopped with a JAM sequence. The TxFIFO address is returned to the beginning of the frame and the state machine goes to state "IFG" to produce the Interframe Gap. The indication that a frame is in the TxFIFO remains set and the frame will be retransmitted when the IFG expires. If the byte count is greater than 64 when the collision occurs, the TxMII logic is instructed to send the JAM sequence and stop the frame transmission. The Control Logic 34 is instructed that the frame has been transmitted. The frame is not retransmitted.

Detailed Description Text (68):
Data is passed from the interfaces 20 and 22 to the MAC logic 24 and 28, respectively, via an 8-bit bus. Therefore, for 100 mbps operation, an 8-bit word of data is available every 80 nanoseconds. If the desired number of ports is 10, the internal clock of the chip can be run with 8 nanosecond cycles. The port selector implemented as a cyclic counter ranges from 0 to 9 or can be implemented to select ports based on a priority or service needed algorithm. In each cycle, a different port is selected. The registers containing state information and frame processing status are replicated for each port. The port selector 46 is used to swap in the state information for the appropriate port to allow cycle processing of that port. At the end of the cycle, the registers are set and stay set until selected again. This process repeats for each port. Once data is accumulated in the receive FIFO or space is available on the transmit FIFO, control information is presented to control logic 34 serving both ports. The control logic will then read or write data from the appropriate FIFO partition to or from the host or network, as the case may

be.

Detailed Description Text (69):
Control information is provided by the TxFIFO and the RxFIFO to Control logic 34 to move data from the host system 12 via host bus 14 and host interface 16 to the TxFIFO, once space is available and transfer data from the RxFIFO to the host system 12, once data is accumulated.

Detailed Description Text (75):
In a step 112, control information is provided by the TxFIFO and an RxFIFO to the control logic, whereupon data is transferred from the RxFIFO to the host system and data is loaded into the TxFIFO from the host system in the sections identified by the port selector and the addresses within the section specified by the Rx or TxMAC, as the case may be.

Detailed Description Text (77):
Summarizing, the present invention describes a multi-port adapter having a single MAC to transfer data in both directions between a host system and a communication network operating on a TDM basis. The MAC has a receive path and a transmit path for processing TDM frames after preliminary processing by a transmit and receive interface, respectively. A port selector selects a register of a state machine for determining the state of the MAC to process data from a selected port. The state machine also identifies a section of a transmit and receive FIFO for storing data in or moving data to the network. The MAC units write the specific address of the data in the FIFO's. Control information is provided by the FIFO's to control logic to transfer data from the receive FIFO to the host system once data is accumulated and transfer data from the transmit FIFO to the network once space is available in the FIFO. The single MAC reduces the circuit count for the adapter as compared to prior art devices using multiple MACs for transferring data.

CLAIMS:

3. The multi-port adapter of claim 2 wherein the storage device is coupled to a host interface and provides instructions to control logic for transmitting and receiving data between the host system and the network.

4. The multi-port adapter of claim 1 further comprising control logic coupled to the storage means and the host system.

13. In a communication network coupled to a multiple port adapter, a Media Access Control chip servicing multiple adapter ports for the network whereby chip logic and size are reduced, comprising:

a) a transmit MAC and a receive MAC in the Media Access Control chip, each MAC coupled at one end to a port multiplexer and at the other end to respective transmit and receive storage registers, the port multiplexer being coupled to the network;

b) transmit and receive state registers coupled to the transmit and receive MACs for tracking the state of each port in the transfer of data in both directions between a host system and the network;

c) control logic coupled to the storage registers and a host interface to control the transfer of data between the host system and the storage registers;

d) a port selector coupled between the multiplexer and the transmit and receive state registers for relating each state register to a port and organizing data in the transmit and receive storage registers on a port basis; and

e) means for activating the port selector to select a different adapter port on a

cyclic basis and provide the state information for the selected port to allow a cycle of processing for that port, at the end of which cycle, the state registers are set and stay set until selected again whereupon processing repeats for each port in a cyclic manner.

16. The system of claim 13 wherein the storage device is coupled to a host interface and provides instructions to the control logic for transmitting and receiving data between the host system and the network.

19. In a communication network coupled to a multiple port adapter, a Single Media Access Control (MAC) coupled to a multiplexer for servicing multiple adapter ports on an individual basis, interface means coupled between the multiplexer and the MAC, a port selector selecting individual ports on a cycle basis, a state machine for tracking the transfer of data between a host system and the network, storage means coupled to the host system and the MAC and control logic for transferring data to and from the host system and the storage means, a method for connecting the MAC to each port on an individual basis for the transfer of data, in both directions, between the host system and the network, comprising the steps of:

a) selecting a port to transfer data between the host system and the network using the port selector;

b) connecting the selected port to the multiplexer and the interface means in a clock cycling;

c) buffering the data in the multiphase to match the speed of the network to the MAC cycle;

d) transmitting a preamble and start frame delimiter in a transmit frame; calculating the frame CRC and signalling any errors in the frame to a physical layer serving the selected port using the interface means;

e) stripping the preamble and start frame delimiter in a received frame; calculating and checking the CRC of the frame, and passing the destination address, source address, type/length field, frame payload to the MAC using the interface means;

f) selecting the state registers for the selected port using the state machine as instructed by the port selector;

g) selecting the section of the storage device to move data out of or store data in using the port selector;

h) processing in the MAC device data provided by the interface means or the storage means and writing data in and/or reading data out of the storage means;

i) updating the state machine on an individual port basis with regard to the data transferred to the network and to the storage device;

j) providing instruction to the control logic for transferring data to/from the storage device and the host system; and

k) repeating steps a)-i) for the next clock cycle.

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Term	Documents
CONTROL	1655138
CONTROLS	571350
LOGIC	255958
LOGICS	2694
(1 AND (CONTROL ADJ1 LOGIC)).USPT.	1
(L1 AND (CONTROL ADJ1 LOGIC)).USPT.	1

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☐ 1. Document ID: US 6373848 B1

L3: Entry 1 of 1 File: USPT Apr 16, 2002

DOCUMENT-IDENTIFIER: US 6373848 B1
TITLE: Architecture for a multi-port adapter with a single media access control (MAC)

Brief Summary Text (21):
These and other objects, features and advantages are achieved in a multi-port adapter chip having a single MAC coupled between a host system and a multi-channel network. The single MAC includes a transmit MAC and a receive MAC path. Each path is coupled at one end through a Media Independent Interface (MII) to a multiplexer and at the other end to separate transmit and receive storage (FIFO) devices. A transmit state machine is coupled to the transmit MAC and transmit FIFO. A receive state machine is coupled to the receive MAC and receive FIFO. The multiplexer is coupled to each port serving a channel through a register and a Physical Layer. Each FIFO is coupled to a host interface and provides instructions to control logic for transmitting and receiving data between the host system and the network. A port selector is coupled to the multiplexer and to the transmit and receive state machines for selecting each port on a cycle basis to transmit and receive data. Each state machine contains a state table having a one word entry for each port in tracking the status of the port. As the ports are selected by the port selector, the associated word for a port is read from the table and used to control the state machine in servicing the port. The port selector also assigns a section in the FIFO's for storing data processed or to be processed by the MACs. The transmit and receive state machines operate concurrently and determine the MAC state for servicing the port, after which the MAC state is updated and stored back into the state table. In the receive direction, the ports are serviced in a round robin fashion. In the transmit direction, data is written into the transmit FIFO as space becomes available. Control Logic means controls the transfer of data between the host system and the network and vice-a-versa when instructed by the FIFOs. The chip architecture is extendable from 10 mbps to 100 mbps and reduces the chip logic by approximately 75% compared to prior art devices.

CLAIMS:

3. The multi-port adapter of claim 2 wherein the storage device is coupled to a host interface and provides instructions to control logic for transmitting and receiving data between the host system and the network.

16. The system of claim 13 wherein the storage device is coupled to a host interface and provides instructions to the control logic for transmitting and receiving data between the host system and the network.

19. In a communication network coupled to a multiple port adapter, a Single Media

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Access Control (MAC) coupled to a multiplexer for servicing multiple adapter ports on an individual basis, interface means coupled between the multiplexer and the MAC, a port selector selecting individual ports on a cycle basis, a state machine for tracking the transfer of data between a host system and the network, storage means coupled to the host system and the MAC and control logic for transferring data to and from the host system and the storage means, a method for connecting the MAC to each port on an individual basis for the transfer of data, in both directions, between the host system and the network, comprising the steps of:

a) selecting a port to transfer data between the host system and the network using the port selector;

b) connecting the selected port to the multiplexer and the interface means in a clock cycling;

c) buffering the data in the multiphase to match the speed of the network to the MAC cycle;

d) transmitting a preamble and start frame delimiter in a transmit frame; calculating the frame CRC and signalling any errors in the frame to a physical layer serving the selected port using the interface means;

e) stripping the preamble and start frame delimiter in a received frame; calculating and checking the CRC of the frame, and passing the destination address, source address, type/length field, frame payload to the MAC using the interface means;

f) selecting the state registers for the selected port using the state machine as instructed by the port selector;

g) selecting the section of the storage device to move data out of or store data in using the port selector;

h) processing in the MAC device data provided by the interface means or the storage means and writing data in and/or reading data out of the storage means;

i) updating the state machine on an individual port basis with regard to the data transferred to the network and to the storage device;

j) providing instruction to the control logic for transferring data to/from the storage device and the host system; and

k) repeating steps a)-i) for the next clock cycle.

Term	Documents
CONTROL	1655138
CONTROLS	571350
LOGIC	255958
LOGICS	2694

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L13: Entry 3 of 8 File: USPT Apr 16, 2002

DOCUMENT-IDENTIFIER: US 6373848 B1
TITLE: Architecture for a multi-port adapter with a single media access control (MAC)

Abstract Text (1):
A multi-port adapter having a single MAC chip has reduced logic circuits for transferring data between a host system and a TDM communication system. The MAC chip includes a transmit MAC and a receive MAC, each coupled at one end to a port multiplexer through an interface and at the other end to respective storage registers. The port multiplexer is coupled to the Physical Layer of each port. Transmit and receive state registers track the state of each port in the transfer of data in the transmit and receive directions. The storage registers are coupled through a host bus interface to a host bus and to the host system. Control logic is coupled to the storage register to control the transfer of data between the system and the storage registers. A port selector coupled between the multiplexer and the transmit and receive state registers selects ports for transfer of data in succession. On each chip clock cycle, the port selector selects a state machine register to determine the state of the MACs for processing the data and a section of the FIFO's to write or read data for the selected port. At the end of the cycle, the state registers are set and stay set until selected again. The process repeats for each port in a cyclic manner. Once data is accumulated in the receive storage register, control logic reads the data of the host bus. Once space is available in the transmit storage register, the control logic writes data from the host system to the transmit storage register.

Brief Summary Text (12):
U.S. Pat. No. 5,293,375 issued Mar. 8, 1994, discloses a repeater interface controller which receives a data packet of one of a plurality of nodes from an associated segment of a Local Area Network (LAN). Each port node includes a partitioning port state machine which monitors its associated segment and partitions a segment from the repeater interface controller when the partitioning port state machine detects a collision in a predetermined number of consecutive data packets. The partitioning port state machine detects collisions in each packet from the beginning of the data packet until the end of a data packet.

Brief Summary Text (13):
U.S. Pat. No. 5,355,375 issued Oct. 11, 1994, discloses a hub controller for providing deterministic access to Carrier-Sense-Multiple-Access (CSMA) Local Area Network. The hub controller includes media control logic that can selectively raise a pseudo-carrier control signal to each port thereby inhibiting any CSMA/collision detection protocol LAN transmissions by that port. In this way, the media control logic allows the hub controller to control which of the multiple ports will be allowed to contend for access to a common internal bus within the hub controller and for how long.

Brief Summary Text (14):
None of the prior art discloses a multi-port adapter having a single MAC and multiplexer to reduce chip logic gates, each port successively coupled to a transmit and receive MAC path using a port selector to identify the port to be serviced and transmit and receive state machines, operating concurrently, to track, transmit and receive status at each port for transfer of data in both directions between a host system and a network.

Brief Summary Text (18):
Another object is a multi-port adapter and method of operation for tracking the

status of each port in transmitting and receiving data between a host system and a network.

Brief Summary Text (19):
Another object is a multi-port adapter and method of operation for selecting a port to transmit and/or receive data between a host system and a network.

Brief Summary Text (20):
Another object is a multi-port adapter and method of operation having a single MAC and multiplexer for transferring data between a host system and a network.

Brief Summary Text (21):
These and other objects, features and advantages are achieved in a multi-port adapter chip having a single MAC coupled between a host system and a multi-channel network. The single MAC includes a transmit MAC and a receive MAC path. Each path is coupled at one end through a Media Independent Interface (MII) to a multiplexer and at the other end to separate transmit and receive storage (FIFO) devices. A transmit state machine is coupled to the transmit MAC and transmit FIFO. A receive state machine is coupled to the receive MAC and receive FIFO. The multiplexer is coupled to each port serving a channel through a register and a Physical Layer. Each FIFO is coupled to a host interface and provides instructions to control logic for transmitting and receiving data between the host system and the network. A port selector is coupled to the multiplexer and to the transmit and receive state machines for selecting each port on a cycle basis to transmit and receive data. Each state machine contains a state table having a one word entry for each port in tracking the status of the port. As the ports are selected by the port selector, the associated word for a port is read from the table and used to control the state machine in servicing the port. The port selector also assigns a section in the FIFO's for storing data processed or to be processed by the MACs. The transmit and receive state machines operate concurrently and determine the MAC state for servicing the port, after which the MAC state is updated and stored back into the state table. In the receive direction, the ports are serviced in a round robin fashion. In the transmit direction, data is written into the transmit FIFO as space becomes available. Control Logic means controls the transfer of data between the host system and the network and vice-a-versa when instructed by the FIFOs. The chip architecture is extendable from 10 mbps to 100 mbps and reduces the chip logic by approximately 75% compared to prior art devices.

Detailed Description Text (3):
Each port 0-N is coupled to a media independent register having separate register portions 16.sup.0 . . . 16.sup.N for handling transmitting data (Tx) and receive data (Rx). The registers 16 .sup.0 . . . 16.sup.N are each coupled to a multiplexer 18 through a transmit (Tx) and a receive (Rx) paths 19, 21, respectively. The multiplexer 18 is key to allowing a single MAC to support multiple ports. The registers are divided into those located in the port's transmit path 19 and those located in the port's receive path 21. The registers located in the transmit path 19 are multiplexed to a transmit interface (TxMII) 20 while the receive registers are demultiplexed through a receive interface RxMII) 22. To match the speed and asynchronous nature of the network clocks and the internal MAC clock there is data buffering in the multiplexer. In the transmit direction there are three bytes of buffer for each port and two bytes of buffer per port in the receive direction.

Detailed Description Text (20):
While in the "JAM" state, the state machine will cause the "jam" sequence to be transmitted. The "jam" sequence is a 32-bit field used to ensure that the collision is detected by all devices attached to the network. When this sequence is being transmitted to the PHY, care must be taken to be sure the PHY can accept the information. If the PHY indicates that it cannot accept the data (Tx_BC inactive) the state machine goes to the "JAM wait" state. When the jam sequence is complete or a reset is received, the state machine will return to the "IDLE" state.

Detailed Description Text (23):
The RxMII is used to strip the Preamble and Start Frame Delimiter (see FIG. 2) from the Ethernet or token ring frames passed to it by the MUX (18). It is also used to calculate and check the CRC for the received frame. The RxMII passes the Destination

address, Source address, Type/Length field, frame payload, and frame CRC to the RxMAC. The IFG is dead time on the network and is thus stripped by the RxMII logic.

Detailed Description Text (24):
The receive interface (RxMII) 22 is coupled to a receive RxMAC 28; a receive state register 30 and the multiplexer 18. The receive interface 22 is used to strip the preamble and Start Frame Delimiter from the frame passed to it by the multiplexer 18. Interface 22 is also used to calculate and check the CRC for the received frame. The interface also passes the destination/length field, frame payload and frame CRC to the RxMAC 28. The IFG portion of the frame is dead time on the network and is stripped by the interface logic. The operation of the interface 22 is described in a state diagram shown in FIG. 4.

Detailed Description Text (59):
In the "IDLE" state the RxMAC is waiting for an indication that a frame is being received by the RxMII logic. When the RxMII logic starts to receive a frame it will assert SOF (start of frame). Detection of SOF by the RxMAC will produce a transition from the "IDLE" state to the "DATA" state. During this transition, the received data byte is written in the RxFIFO and the FIFO address is incremented. It is possible to design the RxMAC logic in such a way that multiple data bytes are written into the RxFIFO with each write operation and the address incremented accordingly. This may be necessary when designing for high speed networks.

Detailed Description Text (67):
Each MAC must process frames received from each of the attached ports. To keep track of the state of each of the ports, each MAC uses the transmit state register 26 and multiplexer 18 for each port and a receive state register 30 and the multiplexer 18 for each port. As the port selector 46 selects a port, the associated transmit and receive state registers are also selected. The transmit state register and multiplexer are used to determine the state of the transmit MAC 24 while the receive state register is used to determine the state of the receive MAC 28 in processing data flowing between the system and the network and vice-versa. The contents of the transmit and receive state registers are updated with new state information as each data byte is transferred between the MAC and the port.

Detailed Description Text (68):
Data is passed from the interfaces 20 and 22 to the MAC logic 24 and 28, respectively, via an 8-bit bus. Therefore, for 100 mbps operation, an 8-bit word of data is available every 80 nanoseconds. If the desired number of ports is 10, the internal clock of the chip can be run with 8 nanosecond cycles. The port selector implemented as a cyclic counter ranges from 0 to 9 or can be implemented to select ports based on a priority or service needed algorithm. In each cycle, a different port is selected. The registers containing state information and frame processing status are replicated for each port. The port selector 46 is used to swap in the state information for the appropriate port to allow cycle processing of that port. At the end of the cycle, the registers are set and stay set until selected again. This process repeats for each port. Once data is accumulated in the receive FIFO or space is available on the transmit FIFO, control information is presented to control logic 34 serving both ports. The control logic will then read or write data from the appropriate FIFO partition to or from the host or network, as the case may be.

Detailed Description Text (70):
In FIG. 9, the single MAC operation begins in a step 100 in which during a system clock cycle, the port selector selects a port 16.sup.0 . . . 16.sup.N to transfer data between the host system and the network on a TDM basis. In a step 102, the port selector connects the multiplexer 18 to the selected port; the Tx interface 20 and the Rx interface 22 during the clock cycle. The Tx interface 20 transmits the preamble and start frame delimiter; calculates the frame CRC and signals any errors to the physical layer. The Rx interface 22 strips the preamble and start frame delimiter from the frame. The Rx interface calculates and checks the CRC for the received frame and passes the destination address, source address, type/length field, frame payload and frame CRC to the RxMAC.

Detailed Description Text (77):
Summarizing, the present invention describes a multi-port adapter having a single

MAC to transfer data in both directions between a host system and a communication network operating on a TDM basis. The MAC has a receive path and a transmit path for processing TDM frames after preliminary processing by a transmit and receive interface, respectively. A port selector selects a register of a state machine for determining the state of the MAC to process data from a selected port. The state machine also identifies a section of a transmit and receive FIFO for storing data in or moving data to the network. The MAC units write the specific address of the data in the FIFO's. Control information is provided by the FIFO's to control logic to transfer data from the receive FIFO to the host system once data is accumulated and transfer data from the transmit FIFO to the network once space is available in the FIFO. The single MAC reduces the circuit count for the adapter as compared to prior art devices using multiple MACs for transferring data.

CLAIMS:

1. A multi-port adapter coupled to a communication network, comprising:

a) a single Media Access Control (MAC) coupled between a host system and through multiple ports operating on a Time Division Multiplex (TDM) basis to each channel of the network;

b) a state machine coupled to the MAC for managing the transfer of information, in both directions between the network and the host on a TDM cycle basis;

c) selector means coupled to the state machine and the multiple ports for selecting each port on a TDM cycle basis to transmit and receive data through the single MAC between the host system and the network; and

d) a multiplexer coupled between the multiple ports and the single MAC, the multiplexer including buffering for matching the speed of the network to the MAC cycling.

3. The multi-port adapter of claim 2 wherein the storage device is coupled to a host interface and provides instructions to control logic for transmitting and receiving data between the host system and the network.

12. The multiport adapter of claim 1 wherein the selector is coupled to a multiplexer and to the state machines for selecting each port on a TDM cycle basis to transmit and receive data between the host system and the network and assigns a section in a storage device for data processed or to be processed by the MAC.

13. In a communication network coupled to a multiple port adapter, a Media Access Control chip servicing multiple adapter ports for the network whereby chip logic and size are reduced, comprising:

a) a transmit MAC and a receive MAC in the Media Access Control chip, each MAC coupled at one end to a port multiplexer and at the other end to respective transmit and receive storage registers, the port multiplexer being coupled to the network;

b) transmit and receive state registers coupled to the transmit and receive MACs for tracking the state of each port in the transfer of data in both directions between a host system and the network;

c) control logic coupled to the storage registers and a host interface to control the transfer of data between the host system and the storage registers;

d) a port selector coupled between the multiplexer and the transmit and receive state registers for relating each state register to a port and organizing data in the transmit and receive storage registers on a port basis; and

e) means for activating the port selector to select a different adapter port on a cyclic basis and provide the state information for the selected port to allow a cycle of processing for that port, at the end of which cycle, the state registers are set and stay set until selected again whereupon processing repeats for each port in a cyclic manner.

15. The system of claim 14 wherein the interface means are state machines implemented in a plurality of states for transferring data, in both directions, between the host system and the network.

16. The system of claim 13 wherein the storage device is coupled to a host interface and provides instructions to the control logic for transmitting and receiving data between the host system and the network.

19. In a communication network coupled to a multiple port adapter, a Single Media Access Control (MAC) coupled to a multiplexer for servicing multiple adapter ports on an individual basis, interface means coupled between the multiplexer and the MAC, a port selector selecting individual ports on a cycle basis, a state machine for tracking the transfer of data between a host system and the network, storage means coupled to the host system and the MAC and control logic for transferring data to and from the host system and the storage means, a method for connecting the MAC to each port on an individual basis for the transfer of data, in both directions, between the host system and the network, comprising the steps of:

a) selecting a port to transfer data between the host system and the network using the port selector;

b) connecting the selected port to the multiplexer and the interface means in a clock cycling;

c) buffering the data in the multiphase to match the speed of the network to the MAC cycle;

d) transmitting a preamble and start frame delimiter in a transmit frame; calculating the frame CRC and signalling any errors in the frame to a physical layer serving the selected port using the interface means;

e) stripping the preamble and start frame delimiter in a received frame; calculating and checking the CRC of the frame, and passing the destination address, source address, type/length field, frame payload to the MAC using the interface means;

f) selecting the state registers for the selected port using the state machine as instructed by the port selector;

g) selecting the section of the storage device to move data out of or store data in using the port selector;

h) processing in the MAC device data provided by the interface means or the storage means and writing data in and/or reading data out of the storage means;

i) updating the state machine on an individual port basis with regard to the data transferred to the network and to the storage device;

j) providing instruction to the control logic for transferring data to/from the storage device and the host system; and

k) repeating steps a)-i) for the next clock cycle.